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PATENT
Attorney Docket No. 4329.3299

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
TSUTOMU SATO ET AL.	)	
	)	
Application No.: 10/820,182	)	Group Art Unit: Unknown
	)	
Filed: April 8, 2004	)	Examiner: Unknown
	)	
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), applicants bring to the attention of the Examiner the documents listed on the attached PTO 1449. This Information Disclosure Statement is being filed within three months of the filing date of the above-referenced application.

Copies of the listed documents are attached.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

The relevance of Japanese Patent Publication No. 2003-31799 is discussed at page 3 of the above-identified application.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: 5/25/04

By: _____
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OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	4329.3299	Appln. No.	10/820,182
Applicant	Sato et al.		
Filing Date	April 8, 2004	Group:	Unknown

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2003-31799	1/31/03	Japan			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Monfray et al., "50nm - Gate All Around (GAA) - Silicon On Nothing (SON) - Devices: A Simple Way to Co-integration of GAA Transistors within bulk MOSFET process," Symposium on VLSI Technology Digest of Technical Papers (2002), pp. 108-109

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce